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GTM

GTM TechDay

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Detroit, Michigan
www.bosch-gtm.com

GTM
overview and motivation

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Agenda

1. Motivation – Why GTM ?
2. Legal Framework – from requirements to products
3. GTM Concept & Architecture
4. GTM Eco-Environment
5. Availability of GTM IP configurations
6. GTM Roadmap & next Gen. GTM

Bosch Reutlingen, Germany – Home of GTM IP Development

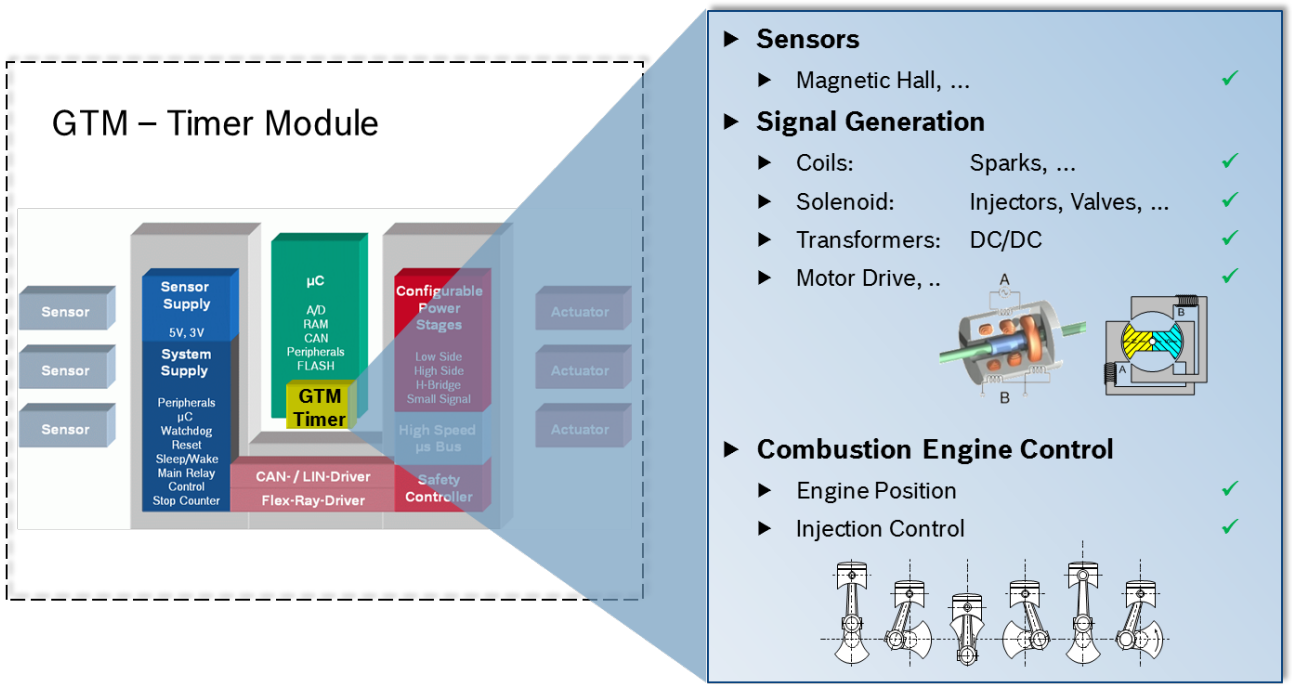
GTM IP - Introduction

Motivation | Why GTM (Gen 1) ?

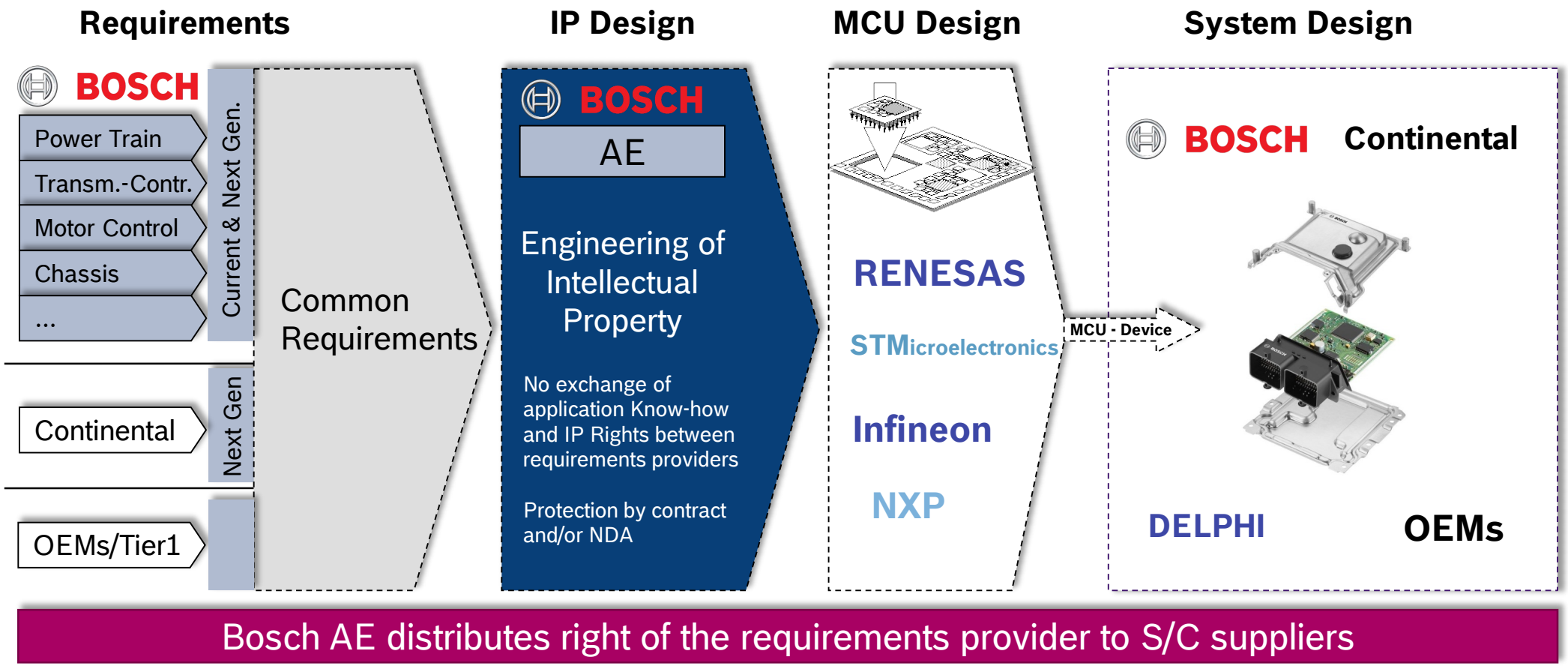
- GTM – Scalable I/O processor platform for …
  - … different application domains (designed for: powertrain, traction control, chassis control, xEV, industry, …)
  - … different classes within one application domain (e.g. 4 cyl. vs 8 cyl. engine)

- Common requirements:
  - Multiple capture/compare of external signals and combination with time stamps
  - Generation of complex output signal waveforms (e.g. PWM signals)
  - Provide common time base for system
  - Minimal CPU interaction / interrupt requests to reduce CPU load

- Application specific requirements:
  - Powertrain needs complex angle clock mechanism
  - Transmission control needs BLDC support



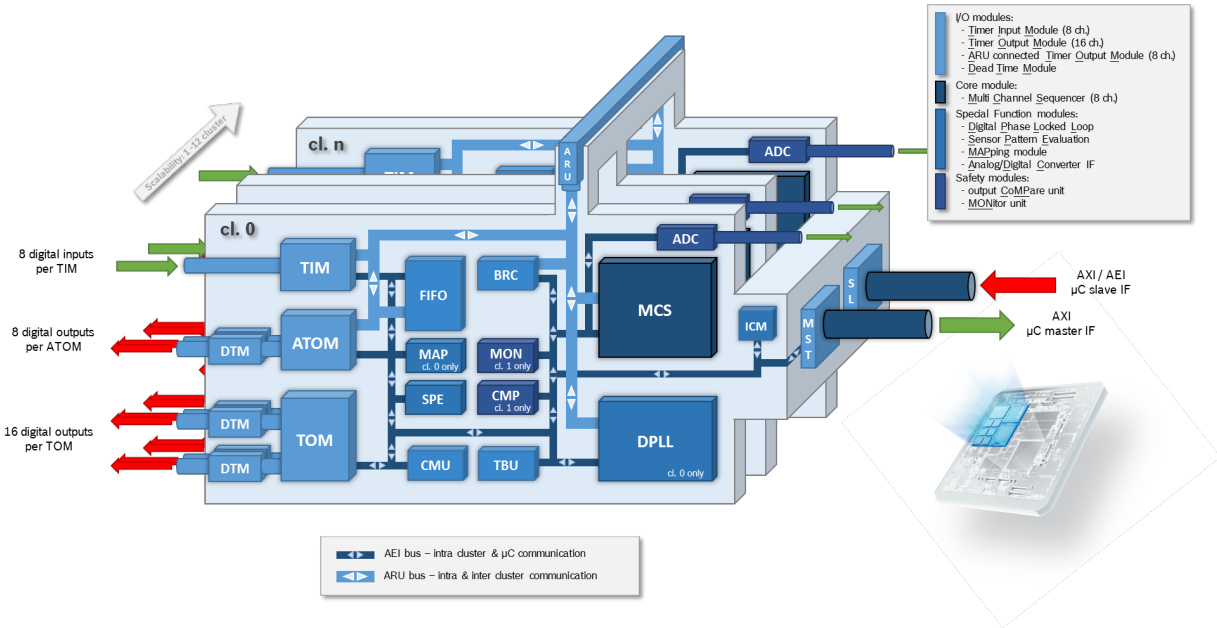
GTM IP - Introduction
Legal framework



GTM IP - Introduction

Concept & Architecture | ... a scalable I/O processor for automotive and industry µCs

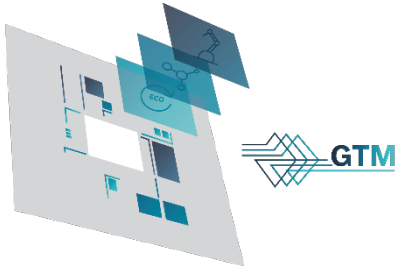
- Programmability by external CPU(s)
- Hardware sub-modules to implement common timer functionality
- Internal core(s) with RISC-like instruction set (MCS)
- Dedicated sub-modules for special functions of different application domains, e.g.:
  - Engine positioning (DPLL)
  - Sensor Evaluation (SPE)
  - Support of safety functions (CMP, MON)
- Central routing unit connects sub-modules and I/O ports in flexible manner
- Optional µC bus master capability to enable workload offloading from µC cores

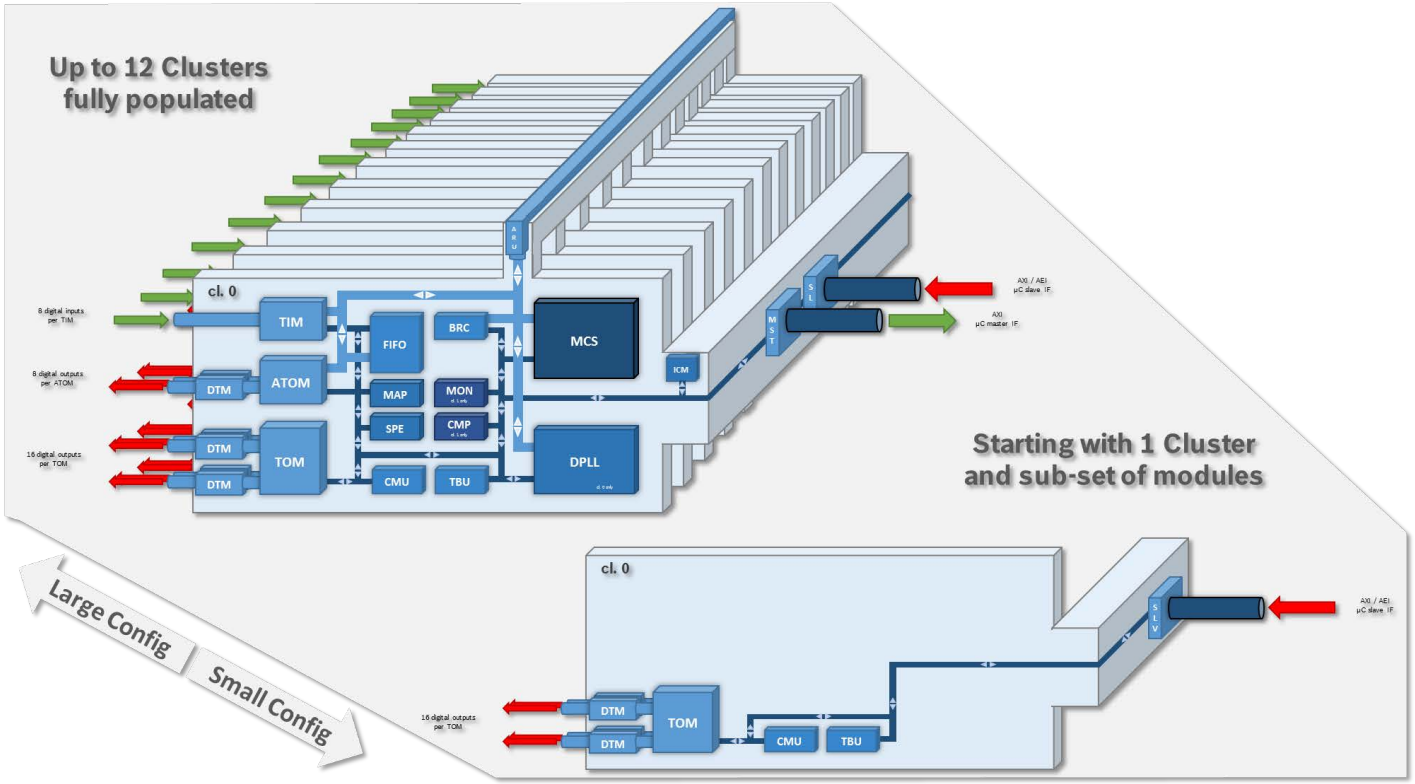


GTM IP - Introduction

Concept & Architecture | ... a scalable I/O processor for automotive and industry µCs

- Highly scalable and modular approach to support wide range of µC & application requirements
  - Low-end support with single instance of basic I/O function modules
    up to
  - High-end support with multiple instances of complex I/O function modules, various special function modules and RISC cores
- Real-time and massive parallel task processing support
- Typical clock frequencies up to 200 MHz



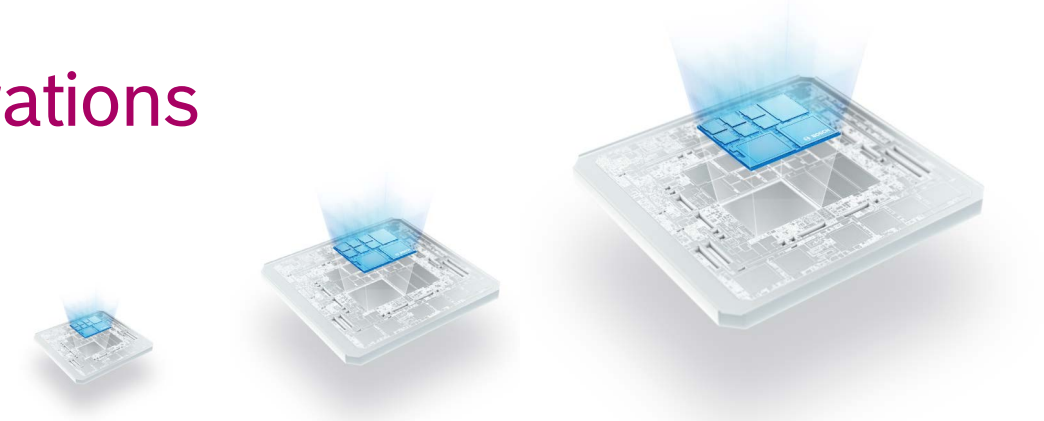


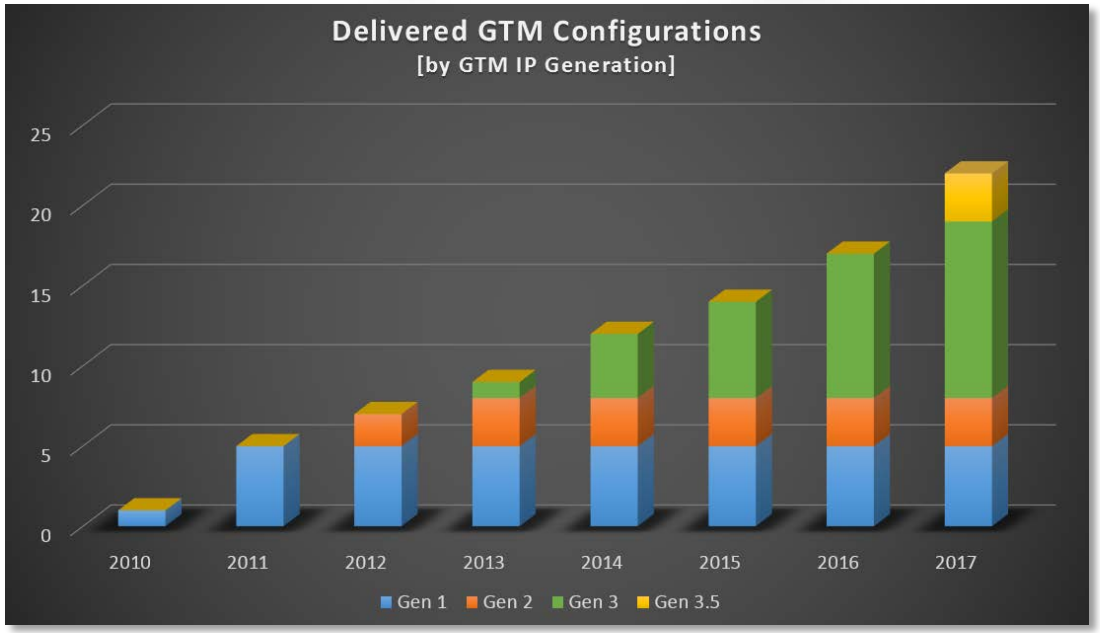
GTM IP - Introduction
Eco Environment

- Continuously growing GTM IP Eco-Environment with support from Bosch as well as various 3rd party companies
  - Rich set of tools and compilers supporting application development including assembler and C compilers for MCS
  - GTM System C Reference Model Support and integration in various virtual MCU prototypes
  - FPGA and emulation support for rapid prototyping of GTM based applications
  - Software drivers and application base library support
  - Debugger Support for efficient development and analysis of GTM applications
  - GTM Training and Application Notes

GTM IP - Introduction
Availability of GTM device configurations

- GTM IP Deliveries
  - First GTM IP (Gen 1) delivery in 2010
  - Meanwhile more than 20 different configurations delivered to multiple semiconductor vendors
  - GTM Gen 3 devices dominating the list with more than 50% of all deliveries
    - GTM Gen 3 incorporates learning and feedback of initial Gen 1 user experiences
    - Major development step vs. Gen 1 & Gen 2
  - Delivery of GTM Gen 3.5 started this year
  - First deliveries on next Gen GTM devices expected to start in 2019
    - Content definition closed
    - Development starting now





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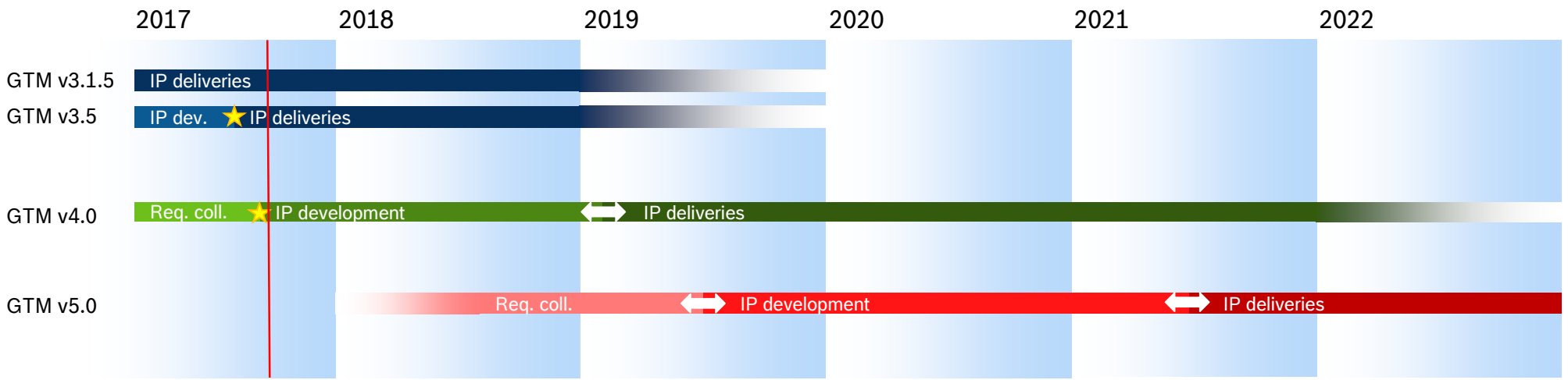
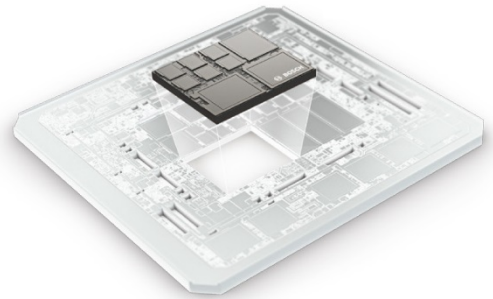
GTM IP - Introduction
RoadMap



- **Gen 3.x** ➔ HighEnd Market | performance & usability
  - Gen 3.5 ➔ NoC Connectivity & Bus-Master Enablement
- **Gen 4.x** ➔ HighEnd Market | efficiency & debug-ability
  - Low-/Mid-Range Market | light & scalable
- **Gen 5.x** ➔ New/Enhanced Feature Set | evolution & revolution



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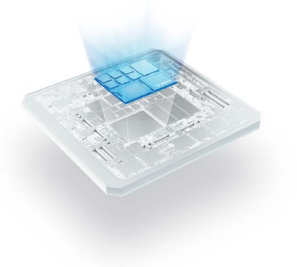
GTM IP Roadmap | GTM Gen 4



- Gen v4.x | available in 2019
  - Improved flexibility of IO module resources
    - Support for light weighted devices with reduced IO feature demand ➔ enables smaller device configurations
    - Dynamic reconfiguration of IO resources for flexible IN/OUT port assignment
  - Improved xEV & non-automotive support
    - Support of new IO and MCS functions required for high efficient support of typical xEV and industry applications
  - Increased compute power
    - MCS architectural upgrade to leverage a higher compute power without breaking backwards compatibility
  - New state-of-the-art build-in GTM/MCS debug support
  - Various upgrades for a more efficient usage of existing GTM functions
    - Incorporating customer feedback for an improved user experience and application efficiency